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Transmitted herewith for filing under 35 U.S.C. 111 and 37 C.F.R. 1.53 is the patent application of:

Hongjiang Song

For: **SYNCHRONIZATION DETECTION ARCHITECTURE FOR SERIAL DATA COMMUNICATION**

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Enclosed are:

- ☒ Certificate of Mailing with Express Mail Mailing Label No. **EL515089467US**
- ☒ **3** sheets of drawings.
- ☐ A certified copy of a application.
- ☒ Declaration ☒ Signed. ☐ Unsigned.
- ☒ Power of Attorney
- ☐ Information Disclosure Statement
- ☐ Preliminary Amendment
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For	#Filed	#Allowed	#Extra		Rate	Fee
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Indep. Claims	3	- 3 =	0	x	$78.00	$0.00
Multiple Dependent Claims (check if applicable) ☐						$0.00
					BASIC FEE	$760.00
					TOTAL FILING FEE	$760.00

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Dated: 12/28/99

Signature

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INTL-0327-US
(P8030)

APPLICATION

FOR

UNITED STATES LETTERS PATENT

TITLE: **SYNCHRONIZATION DETECTION ARCHITECTURE FOR SERIAL DATA COMMUNICATION**

APPLICANT: **HONGJIANG SONG**

Express Mail No.: EL515089467US
Date: December 28, 1999

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SYNCHRONIZATION DETECTION ARCHITECTURE FOR SERIAL DATA COMMUNICATION

BACKGROUND

The invention generally relates to a synchronization detection architecture for serial data communication.

A repeater may be used to relay data between two serial buses. In this manner, a repeater 5 (see Fig. 1) may receive signals (from a serial bus 10) that indicate data and generate signals on another serial bus 20 to relay the data between the buses 10 and 20. In the course of its operation, the repeater 5 sorts out valid data from noise to ensure the integrity of the communications between the two serial buses 10 and 20.

More particularly, the repeater 5 may include a receiver 12 to receive data from the serial bus 10 and a transmitter 14 to communicate data to the serial bus 20. In this manner, the receiver 12 may include a data recovery circuit (DRC) 16 to recover data from the signals that are received from the serial bus 10. Besides recovering data from the serial bus 10, the data recovery circuit 16 typically queues, or buffers, the received data to accommodate the difference between the rate at which the data is received from the serial bus 10 and the rate at which the transmitter 14 communicates data to the serial bus 20.

The data typically is communicated over the serial bus 10, 20 in data packets, or frames. The beginning of a particular frame is marked by a predetermined bit pattern called a start, or synchronization, field, and the repeater 5 may monitor the incoming data to detect the synchronization field to identify a valid frame. In this manner, the repeater 5 does not enable the transmitter 14 to communicate a frame to the serial bus 20 until the repeater 5 has detected the synchronization field that is associated with that frame.

To detect the synchronization field, the receiver 12 may include a synchronization detection circuit 18 that receives recovered bits from the data recovery circuit 16. In this manner, the synchronization detection circuit 18 monitors the recovered bits (from the data recovery circuit 16) to detect the synchronization field, and once detected, the synchronization circuit 18 enables (via a signal line 24) the transmitter 14 to communicate the associated frame to the serial bus 20. This frame includes the recovered bits of data that form the synchronization field and the proceeding recovered bits of data that form the

remainder of the frame. Therefore, all bits of data that are recovered by the data recovery circuit 16 typically passes through the synchronization circuit 18 and then through the transmitter 14 before being communicated to the serial bus 20.

Unfortunately, because all data passes through the synchronization circuit 18, a significant delay may be introduced by the synchronization detection circuit 18, and this delay is in addition to any delay that is introduced by the data recovery circuit 16. For a chain of the repeaters 5, the delays that are introduced by each repeater 5 accumulate and may have a significant impact to the overall system performance. Furthermore, bits may be lost during the repeating process, and as a result, a new synchronization field may have to be regenerated for the retransmission of some frames.

Thus, there is a continuing need for an arrangement that addresses one or more of the problems that are stated above.

SUMMARY

In an embodiment of the invention, a method includes receiving an indication of incoming data from a first serial bus and buffering the bits to accommodate a difference between a first rate of the incoming data and a second rate of outgoing data. During the buffering, the method includes detecting if at least some of the bits indicate a synchronization field.

Advantages and other features of the invention will become apparent from the following drawing, from the description and claims.

BRIEF DESCRIPTION OF THE DRAWING

Fig. 1 is a schematic diagram of a repeater of the prior art.

Fig. 2 is a schematic diagram of a repeater according to an embodiment of the invention.

Fig. 3 is a schematic diagram of a data recovery circuit of the repeater of Fig. 2 according to an embodiment of the invention.

Fig. 4 is a schematic diagram of a coarse adjustment delay line of the data recovery circuit of Fig. 3 according to an embodiment of the invention.

DETAILED DESCRIPTION

Referring to Fig. 2, an embodiment 30 of a serial bus repeater in accordance with the invention includes a serial bus receiver 33 and a serial bus transmitter 40. The receiver 33 is coupled to a serial bus 32 and may receive, for example, one or more signals that indicate bits of data, and when enabled (as described below), the transmitter 40 generates one or more signals on a serial bus 50 to relay this data.

Serial buses typically are subject to noise and thus, the serial bus communications may be effected by a noisy environment. To minimizing the effects of noise, the repeater 28 includes at least two features to ensure reliable data communication. In particular, the repeater 28 includes a synchronization detection circuit 38 to detect a synchronization field, a bit field used to indicate the beginning of a frame of data, and a squelch circuit 35 to determine whether voltages on the serial bus 32 are indicative of noise or indicate logical levels of data bits. If valid data is being received (as indicated by the squelch circuit 35) and the synchronization detection circuit 38 detects a synchronization field, then the transmitter 40 is enabled to communicate the associated frame of data, a frame that includes the bits of the detected synchronization field and the bits that follow the synchronization field and form the remainder of the frame.

In a conventional repeater, bits of data that indicate a synchronization field pass through a data recovery circuit and then pass through a synchronization detection circuit, an arrangement that may introduce a significant latency. Unlike the conventional repeater, to detect the synchronization field, the synchronization detection circuit 38 monitors incoming data while the data is propagating through a data recovery circuit 34 (of the repeater 30) thereby reducing the overall latency that may otherwise be introduced by the receiver 30. Thus, due to this arrangement, the overall latency that is introduced by the repeater 30 is the greater of the delay that is introduced by the data recovery circuit 34 or the delay that is introduced by the synchronization detection circuit 38.

In this course of its operation, the data recovery circuit 34 receives one or more signals from the serial bus 32 and converts these signals into indications of bits of data. The data recovery circuit 34 may queue, or buffer, this incoming data for purposes of accommodating different data rates between the incoming data and the outgoing data that is communicated over the serial bus 50. In this manner, if the incoming data is being received

at a rate that is higher than the rate at which the transmitter 40 is communicating outgoing data to the serial bus 50, then the data recovery circuit 34 buffers the incoming bits to compensate for the different rates. In some embodiments, while the data recovery circuit 34 is buffering the incoming data, the synchronization detection circuit 38 monitors the buffered data to detect a bit pattern that indicates the synchronization field.

When the synchronization detection circuit 38 detects the synchronization field, the circuit 38 enables the transmitter 40 to communicate the frame that is associated with the synchronization field over the serial bus 50. In this manner, in some embodiments, after the transmitter 40 communicates a particular frame over the serial bus 50, the transmitter 40 is not again enabled to transmit again until both the synchronization detection circuit 38 indicates the detection of another synchronization field and the squelch circuit 35 indicates that valid logical levels are present on the serial bus 32. When these two conditions occur, the transmitter 40 is enabled to communicate the frame that is associated with the detected synchronization field to the serial bus 50.

In some embodiments, once enabled to transmit, the transmitter 40 receives the bits of the synchronization field (from the data recovery circuit 34) before the other bits of the frame. Thus, the transmitter 40 does not regenerate the synchronization field, but instead, the transmitter 40 relays the buffered synchronization field to the serial bus 50. The transmitter 40 then receives the remaining bits of the frame and communicates these bits to the serial bus 50.

Referring to Fig. 3, in some embodiments, the data recovery circuit 34 may include an analog-to-digital (A/D) interface 60 that receives a clock signal (called CLK_1) from a clock line of the serial bus 32 and other signals from data lines of the serial bus 32. In this manner, on each cycle of the CLK_1 signal, the A/D interface 60 samples and converts two analog data signals from the serial bus 32 into two bits that are received by a fine adjustment delay line 63. The delay line 63 delays the bits to adjust the phase between the CLK_1 clock signal of the serial bus 32 and the CLK_2 clock signal of the serial bus 50. The phase adjusted bits subsequently pass into a coarse adjustment delay line 65, a delay line that delays the bits by a multiple number of CLK_2 cycles to accommodate an overall difference in the data rates between the incoming and outgoing data serial buses 32 and 50. In this manner, the coarse adjustment delay line 65 queues, or buffers, the incoming bits to approximately match the

rate at which the data is available for transmission to the rate at which the transmitter 40 is communicating the data to the serial bus 50. In some embodiments, a digital signal processing (DSP) engine 62 (of the data recovery circuit 34) adjusts (via control lines 64) the delays that are introduced by the fine adjustment delay line 63 and the coarse adjustment delay line 65.

Referring also to Fig. 4, in some embodiments, the coarse adjustment delay line 65 includes registers 70 (registers 70_1, 70_2, . . . 70_{N-1} and 70_N, as examples), each of which may be used to introduce a delay of one CLK_2 clock cycle. As an example, each register 70 may be a D-type flip-flop. In some embodiments, the registers 70 are serially coupled together to form a first-in-first-out (FIFO) that has a fixed output pointer and an adjustable input pointer to allow adjust of the coarse delay. More particularly, in some embodiments, the registers 70 are serially coupled together in the following order: register 70_1 to 70_2 . . . to 70_{N-1} to 70_N, with the output terminals 45 of the register 70_N forming output terminals 42 of the coarse delay line 34. The input terminals of each register 70 are coupled to the output terminals of an associated multiplexer 69. In this manner, one set of input terminals of each multiplexer 69 is coupled to input lines 67 of the delay line 65, and another set of input terminals of each multiplexer 69 (the multiplexer 69 that is associated with the register 70_1 being the exception) is coupled to the output terminals 45 of the preceding register 70. The select terminals of the multiplexers 69 are coupled to the control lines 64. Due to this arrangement, the DSP engine 62 may use the control lines 64 to select which register 70 receives the input signals from the lines 67 and thus, control the input pointer in this manner.

The DSP engine 62 adjusts the coarse delay by moving the input pointer of the FIFO. For example, the DSP engine 62 may adjust the input pointer to store the data from the fine adjustment delay line 63 in the registers 70_{N-1} and thus, introduce a two clock (the CLK_2 clock) delay in the propagation of the incoming data through the coarse delay line 65. As another example, the DSP engine 62 may move the input pointer to provide the data from the fine adjustment delay line 63 to the first register 70_1 of the FIFO to introduce the maximum delay to the data.

The synchronization detection circuit 38 is coupled to a contiguous block of the registers 70 to detect the synchronization field. For example, the synchronization detection circuit 38 may be coupled to output terminals 45 of a contiguous group of registers 70 that

includes the last register 70_N. As an example, the synchronization detection circuit 38 may include a digital comparator that compares the signals that are provided by the terminals 71 of a selected group of the registers 70 with a predetermined bit pattern. Based on the result of the comparison, the comparator either asserts (drives high, for example) or deasserts (drives low, for example) the line 24 for purposes of selectively enabling or disabling the transmitter 40.

While the invention has been disclosed with respect to a limited number of embodiments, those skilled in the art, having the benefit of this disclosure, will appreciate numerous modifications and variations therefrom. It is intended that the appended claims cover all such modifications and variations as fall within the true spirit and scope of the invention.

What is claimed is:

1. A method comprising:

receiving an indication of bits of incoming data from a first serial bus;

buffering the bits to accommodate a difference between a first rate of the incoming data and a second rate of outgoing data;

during the buffering, detecting whether at least some of the bits indicate a synchronization field.

2. The method of claim 1, further comprising:

after the buffering, communicating the bits to a second serial bus to form the outgoing data.

3. The method of claim 2, wherein the communicating comprises:

selectively enabling a transmitter based on the detection.

4. The method of claim 3, further comprising:

determining whether the indication of the bits indicates valid bit logic levels; and

further basing enablement of the transmitter on the determination.

5. The method of claim 1, wherein the receiving comprises:

receiving an indication of at least one analog signal from the first serial bus; and

converting the indication of said at least one analog signal into indications of at least some of the bits.

6. The method of claim 1, wherein the buffering comprises:

passing the bits through a delay line.

7. The method of claim 1, wherein the detecting comprises:

comparing at least some of the bits to an indication of a predetermined bit pattern.

8. A repeater comprising:

a data recovery circuit to receive an indication of bits of incoming data from a first serial bus and buffer the bits to accommodate a difference between a first rate of the incoming data and a second rate of outgoing data; and

a synchronization detection circuit coupled to the data recovery circuit to detect, while the data recovery circuit buffering the bits, whether at least some of the bits indicate a synchronization field.

9. The repeater of claim 8, further comprising:

a transmitter to receive an indication of the bits from the data recovery circuit and use the indication from the data recovery circuit to communicate the bits to a second serial bus to form the outgoing data.

10. The repeater of claim 9, wherein the synchronization circuit selectively enables the transmitter based on the detection by the synchronization detection circuit.

11. The repeater of claim 10, further comprising:

a squelch detection circuit to indicate whether valid bit logic levels are present on the first serial bus,

wherein the synchronization circuit selectively enables the transmitter further based on the indication from the squelch detection circuit transmitter.

12. The repeater of claim 10, further comprising:

an analog-to-digital conversion circuit to receive an analog signal from the first serial bus and convert the analog signal into an indication of at least some of the bits.

13. The repeater of claim 10, wherein the data recovery circuit comprises:

a delay line to delay the bits by multiple cycles of a clock signal.

14. The repeater of claim 10, wherein the synchronization detection circuit comprises:

a comparator to compare at least some of the bits to an indication of a predetermined bit pattern to perform the detection.

15. A system comprising:

a first serial bus;

a second serial bus; and

a repeater coupled to the first and second serial busses to receive an indication of bits of incoming data from the first serial bus, and concurrently buffer the bits to accommodate a difference between a first rate of the incoming data and a second rate of outgoing data and detect whether at least some of the bits indicate a synchronization field.

16. The system of claim 15, wherein the repeater comprises:

a receiver to receive an indication of bits of the incoming data from the first serial bus; and

a transmitter to communicate the bits to a second serial bus to form the outgoing data.

17. The system of claim 16, further comprising:

a synchronization circuit to detect the synchronization field and selectively enable the transmitter in response to the detection.

18. The synchronization circuit of claim 16, wherein the synchronization detection circuit comprises:

a comparator to compare at least some of the bits to an indication of a predetermined bit pattern to perform the detection.

19. The system of claim 15, further comprising:

a squelch detection circuit to enable communication to the second serial bus based on whether valid bit logic levels are present on the first serial bus.

20. The system of claim 15, further comprising:

an analog-to-digital conversion circuit to receive an analog signal from the first serial bus and convert the analog signal into an indication of at least some of the bits.

SYNCHRONIZATION DETECTION ARCHITECTURE FOR SERIAL DATA COMMUNICATION

ABSTRACT OF THE DISCLOSURE

A method includes receiving an indication of incoming data from a first serial bus and buffering the bits to accommodate a difference between a first rate of the incoming data and a second rate of outgoing data. During the buffering, the method includes detecting if at least some of the bits indicate a synchronization field.

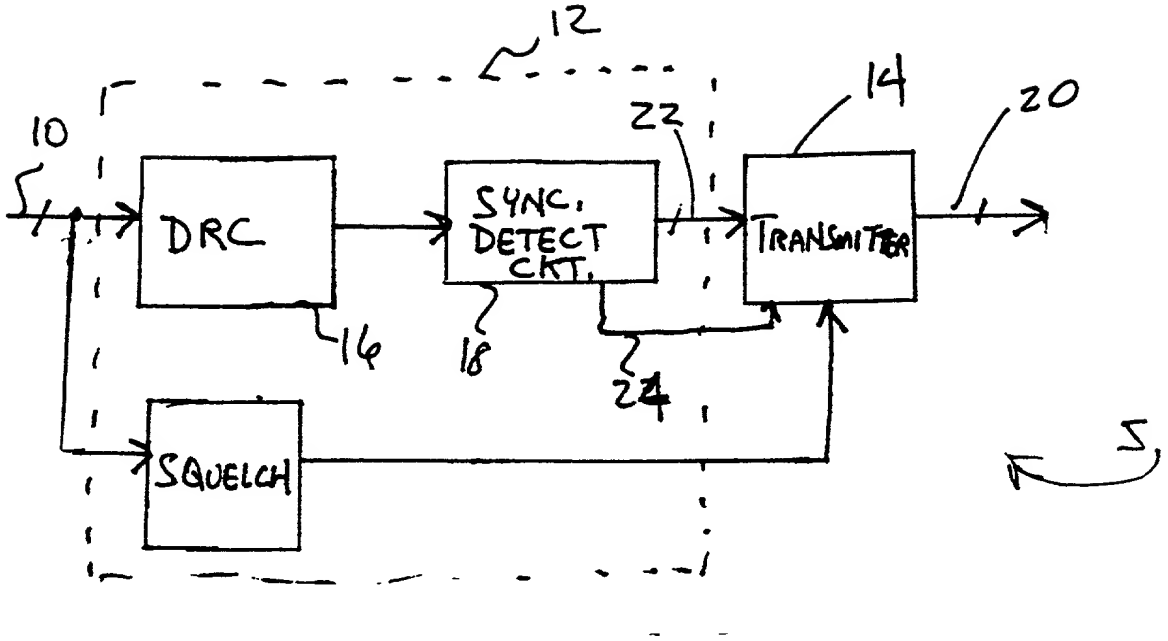


FIG. 1 (PRIOR ART)

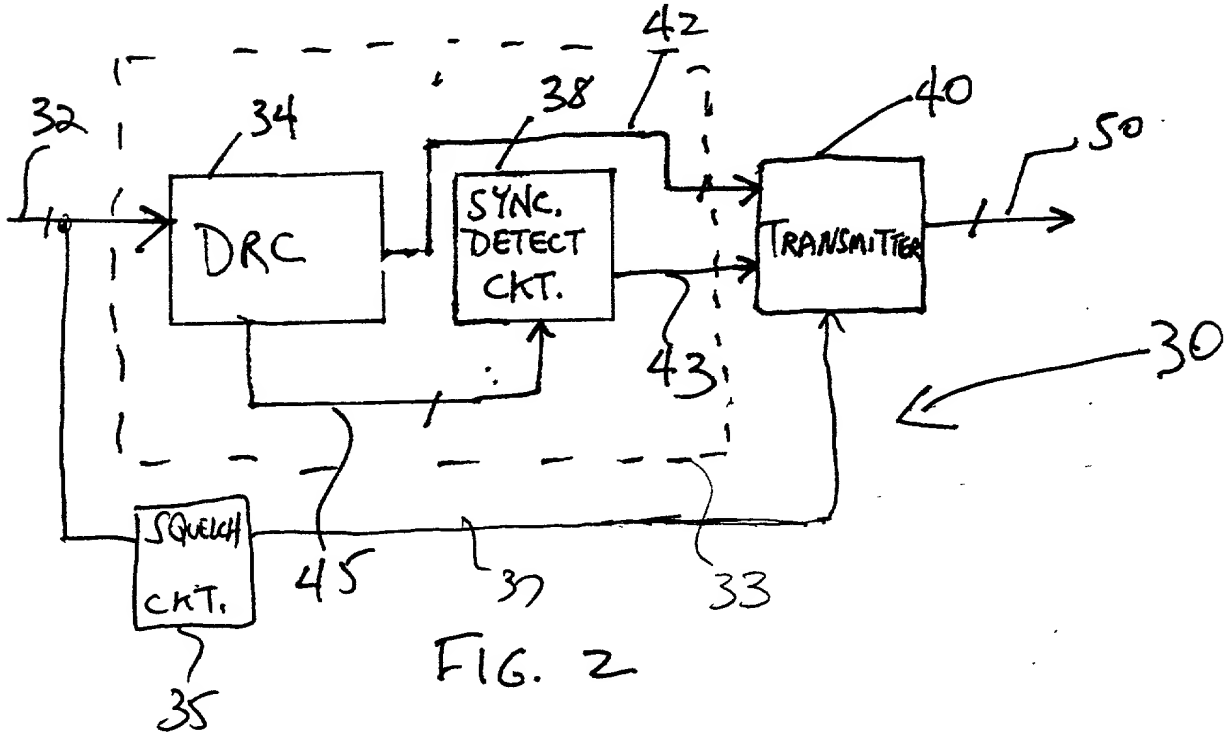
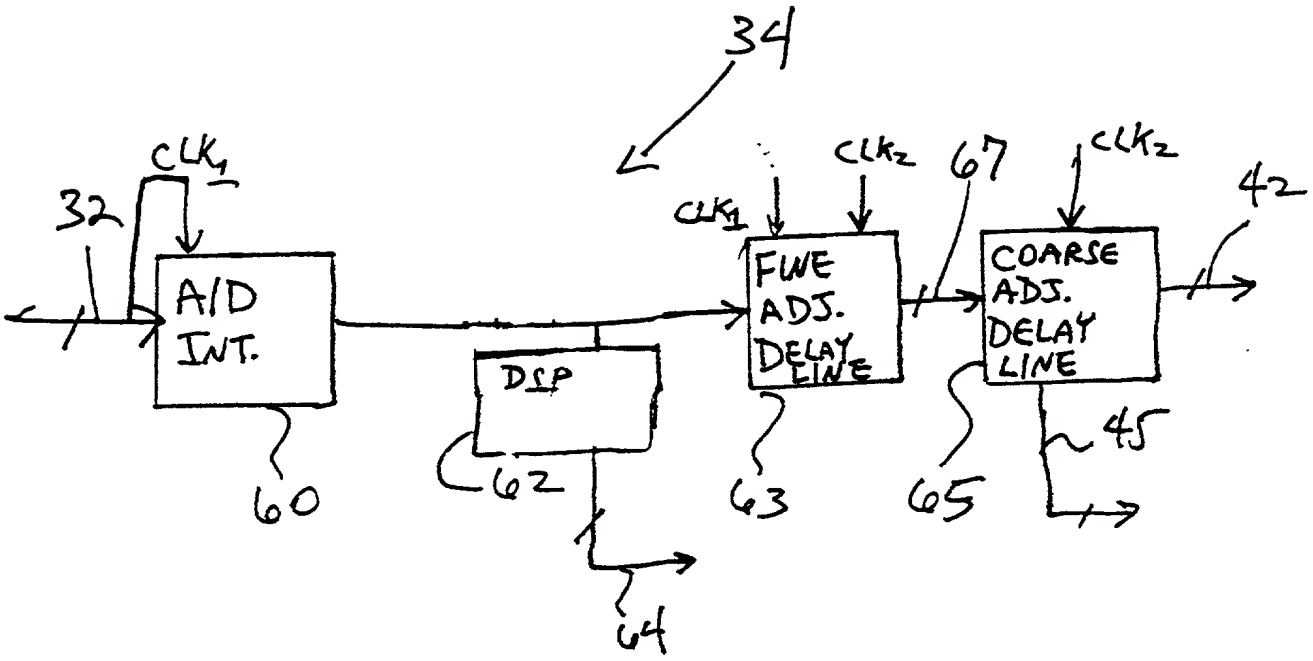


FIG. 2


34
CLK1
32
A/D
INT.
60
DSP
62
64
CLK1
CLK2
FINE
ADJ.
DELAY
LINE
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67
CLK2
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ADJ.
DELAY
LINE
65
42
45

FIG. 3

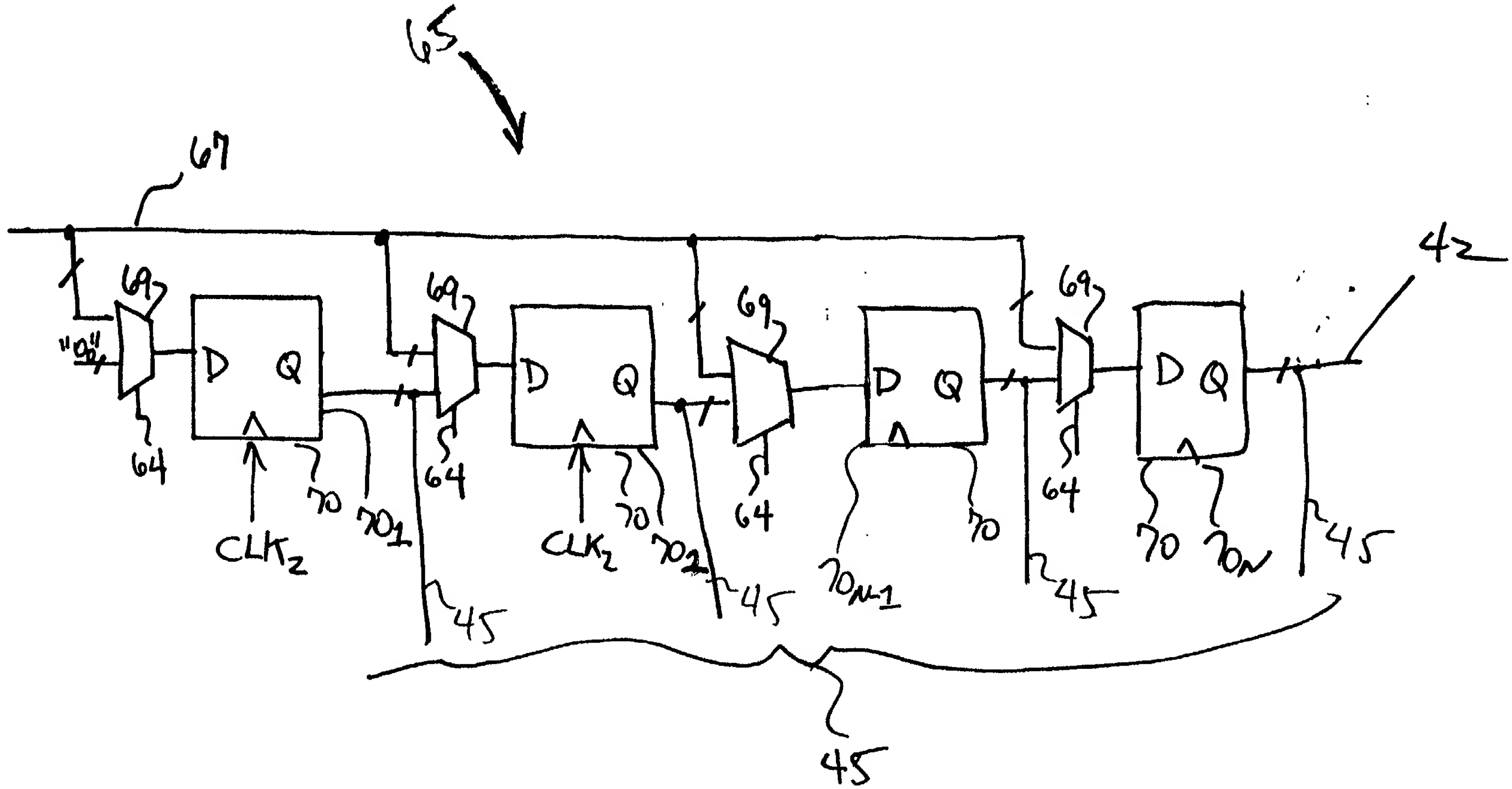

FIG. 4

Attorney's Docket No.: INTL-0327-US (P8030) PATENT

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

SYNCHRONIZATION DETECTION ARCHITECTURE
FOR SERIAL DATA COMMUNICATION

the specification of which

X	is attached hereto.
	was filed on _____ as
	United States Application Number _____
	or PCT International Application Number _____
	and was amended on _____
	(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate Issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):			Priority Claimed	
Number	(Country)	(Day/Month/Year Filed)	Yes	No
Number	(Country)	(Day/Month/Year Filed)	Yes	No

Number	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under title 35, United States Code, Section 119(e) of the United States provisional application(s) listed below:

(Application Number)	(Filing Date)
(Application Number)	(Filing Date)

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

(Application Number)	Filing Date	(Status-patented, pending, abandoned)
(Application Number)	Filing Date	(Status-patented, pending, abandoned)

I hereby appoint Timothy N. Trop, Reg. No. 28,994; Fred G. Pruner, Jr., Reg. No. 40,779, Dan C. Hu, Reg. No. 40,025; Coe F. Miles, Reg. No. 38,559, and John R. Merkling, Reg. No. 31,716 my patent attorneys, of TROP, PRUNER, HU & MILES, P.C., with offices located at 8554 Katy Freeway, Ste. 100, Houston, TX 77024, telephone (713) 468-8880, and Joseph R. Bond, Reg. No. 36,458; Richard C. Calderwood, Reg. No. 35,468; Sean Fitzgerald, Reg. No. 32,027; David J. Kaplan, Reg. No. 41,105; Leo V. Novakoski, Reg. No. 37,198; Naomi Obinata, Reg. No. 39,320; Thomas C. Reynolds, Reg. No. 32,488; Steven P. Skabrat, Reg. No. 36,279; Howard A. Skaist, Reg. No. 36,008; Steven C. Stewart, Reg. No. 33,555; Raymond J. Werner, Reg. No. 34,752; and Charles K. Young, Reg. No. 39,425; my patent attorneys, of INTEL CORPORATION; with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to Timothy N. Trop, TROP, PRUNER, HU & MILES, P.C., 8554 Katy Freeway, Ste. 100, Houston, TX 77024 and direct telephone calls to Fred G. Pruner, (713) 468-8880.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Post Office Address: **4145 W. DUBLIN ST., CHANDLER, AZ 85226**	